PORTING CONSIDERATIONS FROM C8051F320/1 AND C8051F326/7 TO C8051F38X

1. Introduction

This application note highlights the differences between the C8051F320/1 or C8051F326/7 and C8051F38x MCU families. These families are largely code-compatible, requiring very minor changes when porting firmware between device families.

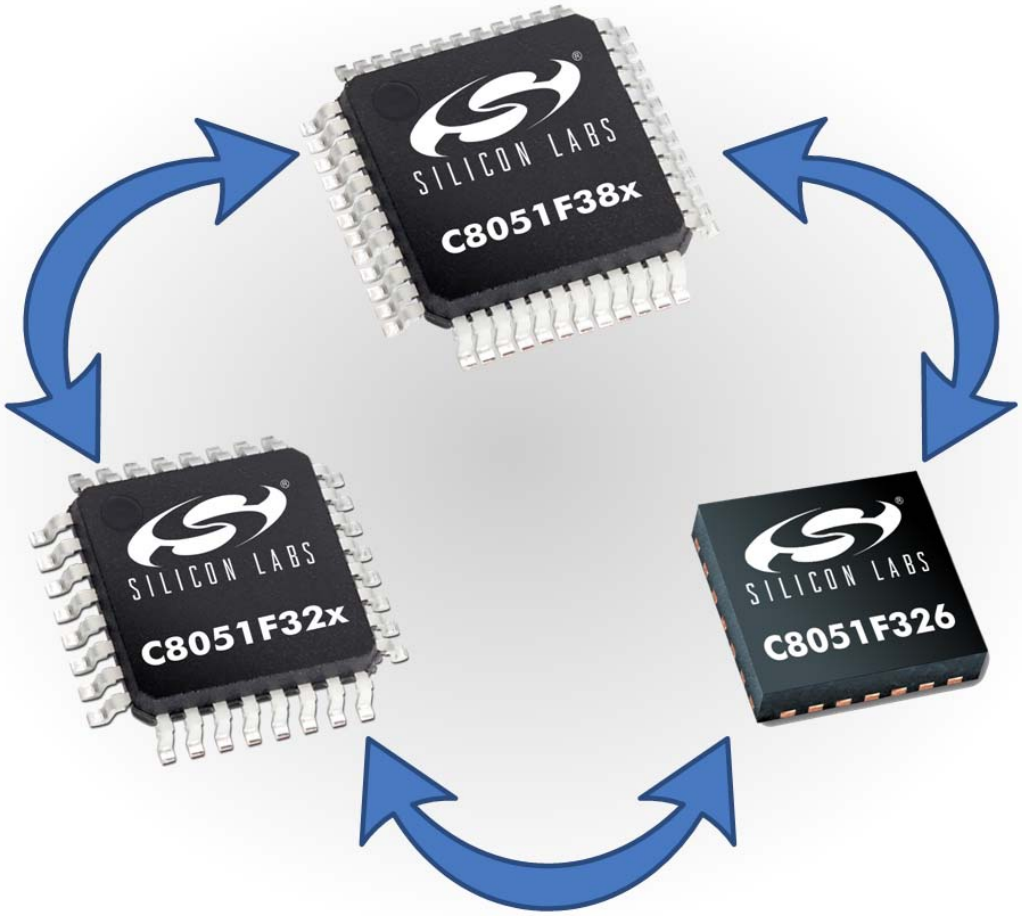


Figure 1. Porting Code Between C8051F320/1, C8051F326/7, and C8051F38x Families

2. Relevant Documentation

Silicon Labs data sheets are available on the specific device landing page:

- **C8051F320/1 Data Sheet** — https://www.silabs.com/products/mcu/usb/Pages/C8051F32x-34x.aspx and click on the **Documentation** tab.
- **C8051F326/7 Data Sheet —** https://www.silabs.com/products/mcu/usb/Pages/C8051F32x-34x.aspx and click on the **Documentation** tab.
- **C8051F38x Data Sheet —** https://www.silabs.com/products/mcu/usb/Pages/C8051F38x.aspx and click on the **Documentation** tab.

3. Distinguishing Features

Table 1 provides a summary for the primary differences among the three MCU families: C8051F320/1, C8051F326/7, and C8051F38x.

Some peripherals and capabilities are unique to one of the families. When moving a design from one MCU family to another, ensure that the new MCU family includes the necessary features. Also, note that the features listed in the table might not be available in all products in the product family. See the applicable data sheet to determine the part number that includes features necessary for the design.

Table 1. Feature Differences Between MCU Families

Feature	C8051F320/1	C8051F326/7	C8051F38x
Core			
XRAM	2304 bytes	1536 bytes	4352 or 2304 bytes
Flash	16 kB	16 kB	64 or 32 kB
Internal Oscillator	24 MHz	24 MHz	48 MHz
SFR Paging	—	—	✓
Analog			
Resolution	10 bits	—	10 bits
Maximum Throughput Rate	200 ksps	—	500 ksps
Comparators	2	—	2
Voltage Reference	External, 2.44 V internal, or VDD pin	—	External, 1.2 V / 2.4 V internal, output of the internal regulator (1.8 V), or VDD pin
Digital			
Port Pins	25/21	15	40/25
UART	1	1	2
SMBus	✓	—	additional hardware acknowledge, and start detection timing
SPI	1	—	1
Timers	4	2	6
Programmable Counter Array	✓	—	✓
External Memory Interface (EMIF)	—	—	✓
Pinout and Packages			
QFN-28 (pin incompatible)	✓	✓	—
QFN-28 (pin compatible)	C8051F327 is pin-compatible with C8051F321, with ‘F321 including additional GPIO		—
LQFP-32 (pin compatible)	✓	—	✓
QFN-32 (5x5 mm)	—	—	✓
TQFP-48	—	—	✓

3.1. Hardware Incompatibilities

While the C8051F38x family includes a number of new features not found on the C8051F320/1 and C8051F326/7 families, there are some fundamental differences that should be considered for any design port.

- Clock Multiplier — The C8051F38x family does not include the 4x clock multiplier from the C8051F320/1 and C8051F326/7 device families. Instead, the internal oscillator is a 48 MHz oscillator that is divided down to the default oscillator frequency. The clock multiplier register is still present and is backwards compatible with the C8051F320/1 and C8051F326/7 oscillator initialization code. This change only impacts systems which use the clock multiplier in conjunction with an external oscillator source.
- External Oscillator C and RC Modes — The C and RC modes of the oscillator have a divide-by-2 stage on the C8051F38x to aid with noise immunity. This was not present on the C8051F320/1 device family, and any clock generated with C or RC mode will change accordingly.
- Fab Technology — The C8051F38x family is manufactured using a different technology process than the C8051F320/1 and C8051F326/7 families. As a result, many of the electrical performance parameters will have subtle differences. These differences should not affect most systems, but it is nonetheless important to review the electrical parameters for any peripherals that are used in the design and ensure they are compatible with the existing hardware.

3.2. Special Function Register Paging

The C8051F38x devices implement a paged special function register (SFR) scheme that greatly expands the number of available SFR addresses. This SFR address expansion provides support for more peripherals, such as:

- Second SMBus peripheral (SMBus1)
- Timer 4 and Timer 5

To correctly read or write to SFRs in a ’F38x device, the SFRPAGE register must be set to the correct SFR page. The SFRPAGE register itself is accessible from all SFR pages. For example, to access the SMBus1 Clock and Configuration register SMB1CF, SFRPAGE must be set to 0x0F:

```
SFRPAGE = CONFIG_PAGE; // Switch SFR page to 0x0F

SMB1CF |= 0x80; // Enable SMBus1
```

CONFIG_PAGE is defined as 0x0F in the **C8051F380_defs.h** header file. It is recommended to use the defined constants for SFRPAGE to enhance code readability and to reduce the porting effort for future platforms.

When porting code from a ’F320/1 or ‘F326/7 device to a ’F38x device, modify the firmware to set the SFRPAGE before any SFR accesses. When porting code from a ’F38x device to ’F320/1 or ‘F326/7 device, remove all writes to SFRPAGE. Alternatively, code can define the same SFR Page defines on the ‘F320/1 and ‘F326/7 and set them all to 0x00 to promote back-and forth compatibility between the two families. For example, **CONFIG_PAGE** is set to 0x0F on the ‘F38x, but can be defined as 0x00 for the ‘F320/1 or ‘F326/7 so no code modifications are needed.

3.3. ADC

The ADC peripheral is different between the C8051F320/1 and C8051F38x families. The C8051F320/1 devices feature a 10-bit, 200 ksps SAR, while C8051F38x devices have a 10-bit, 500 ksps SAR. Table 2 details the list of differences that may affect the system and code design.

Table 2. Feature Differences Between MCU Families

Feature	C8051F320/1	C8051F38x
Resolution	10 bits	10 bits
Maximum Throughput Rate	200 ksps	500 ksps
Maximum SAR Conversion Clock	3 MHz	8.33 MHz
Power Supply Current (VDD supplied to ADC0)	400 µA (200 ksps)	750 µA (500 ksps)

3.4. External Data Memory Interface (EMIF)

An External Memory Interface (EMIF) is available on the C8051F380/2/4/6 devices and can be used to access off-chip data memories and memory-mapped devices connected to the GPIO ports. The external memory space may be accessed using the external move instruction (MOVX) and the data pointer (DPTR) or using the MOVX indirect addressing mode using R0 or R1.

3.5. Voltage Reference

The C8051F380/1/2/3 devices also include an on-chip voltage reference circuit which consists of a 1.2 V, temperature stable band gap voltage reference generator and a selectable-gain output buffer amplifier. The buffer is configured for 1x or 2x gain using the REFBGS bit in register REF0CN. On the 1x gain setting, the output voltage is nominally 1.2 V, and on the 2x gain setting, the output voltage is nominally 2.4 V.

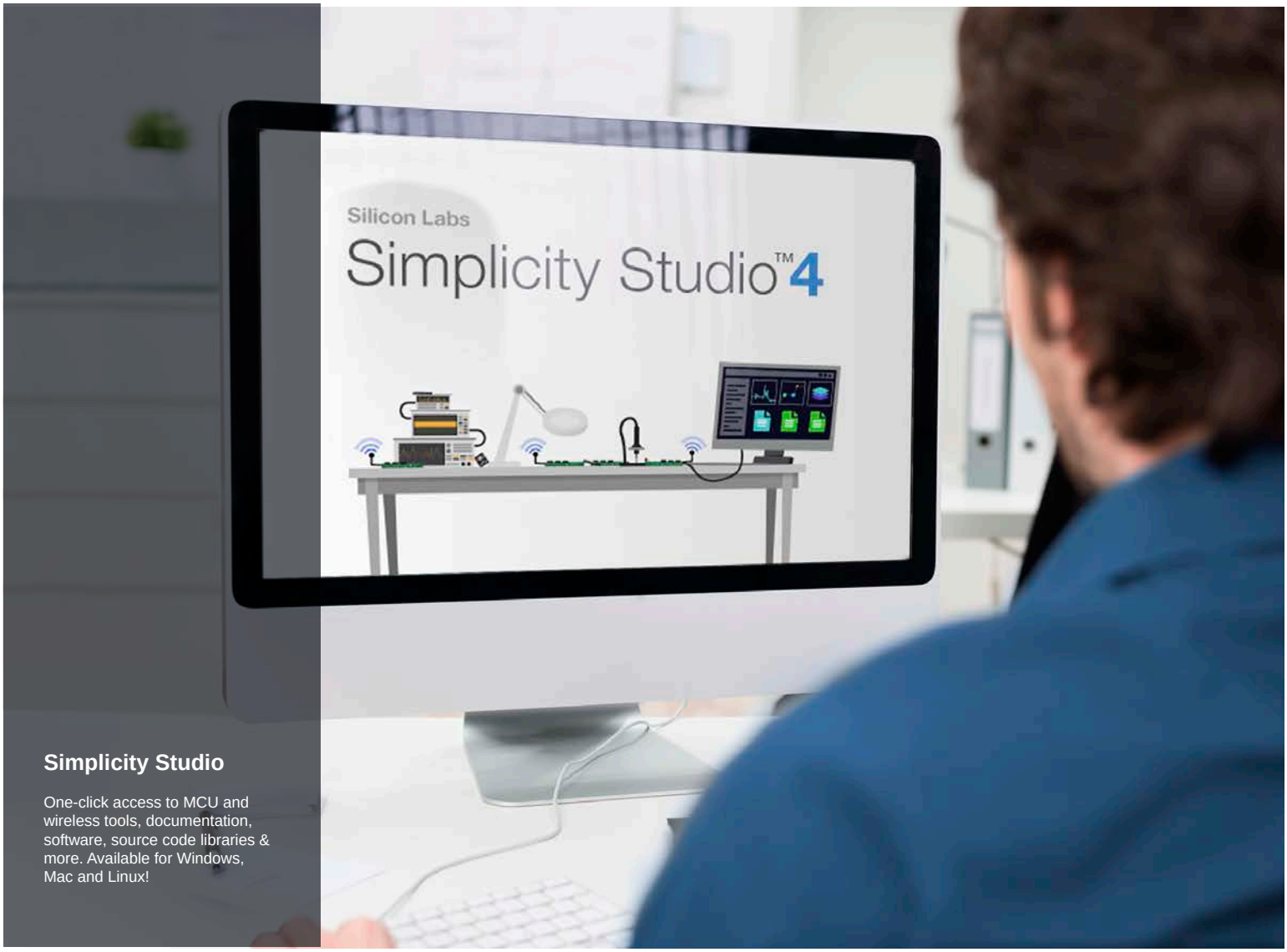
3.6. Other Peripherals

All other peripherals and features not discussed in the previous sections are functionally the same among the three device families. If SFR paging is accounted for, firmware written for these peripherals will operate the same way on any of the three device families.

3.7. Pinout and Packages

Devices in the C8051F320/1 and C8051F38x families are pin-compatible in the LQFP-32 package. C8051F38x devices are also available in QFN-32 (5x5 mm) or TQFP-48 packages.

The C8051F327 (QFN-28) is pin-compatible with the C8051F321 device, though the C8051F321 has additional GPIO pins. If these pins are in use, an application using the C8051F321 may not be able to migrate to the C8051F327 device. The C8051F326 is also in a QFN-28 package but is not compatible with the C8051F321. The C8051F320 LQFP-32 package is not pin-compatible with the C8051F326/7 devices.



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